

TRAN - 249 US P

UNITED STATES PATENT APPLICATION
For

DEEP N-WELL CAPACITOR

Inventors:

Robert Paul Masleid
James B. Burr

Prepared by:
WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CALIFORNIA 95113
(408) 938-9060

DEEP N-WELL CAPACITOR

FIELD OF THE INVENTION

Embodiments in accordance with the present invention relate to systems
5 and methods for adding capacitance to an integrated circuit.

BACKGROUND

Highly integrated semiconductor devices, e.g., microprocessors, are limited to a maximum frequency of operation that is in large part limited by transient
10 current capabilities of the integrated circuit packaging. For example, an integrated circuit package introduces too much power supply inductance for the integrated circuit to achieve a desired operating frequency. The conventional art utilizes discrete capacitors within the packaging and explicitly constructed gate oxide capacitors. Such dedicated gate capacitors require a relatively large
15 integrated circuit area, and are prohibitively expensive to achieve sufficient decoupling capacitance. Adding capacitors to the packaging incurs a deleterious increase in packaging cost and complexity, while decreasing reliability.

Summary of the Invention

Therefore, a system of adding capacitance to an integrated circuit without sacrificing circuit area would be highly desirable.

5

Accordingly, a deep n well capacitor is disclosed. A deep n well is formed in an integrated circuit. The deep n well can be parasitically coupled to Vdd and ground in one example. A reverse-biased diode depletion region forms between n type and p type material, creating a capacitor. The capacitor provides local, on-10 chip decoupling of power supplied to active transistor devices on the integrated circuit, enabling greater operating frequencies for the integrated circuit.

In accordance with other embodiments of the present invention, multiple layers of deep n well can be configured as deep n well capacitors, increasing 15 capacitance available in the integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a side-sectional view of an integrated circuit comprising deep n-well capacitor structure, in accordance with embodiments of the present invention.

5

Figure 2A illustrates using the same mask to form both a first and a second deep n well, in accordance with embodiments of the present invention.

10 Figure 2B illustrates a second deep n well layer formed using a different mask than a first deep n well layer, in accordance with embodiments of the present invention.

15 Figure 3 illustrates a flow chart for a method of high frequency operation in an integrated circuit, in accordance with embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the present invention, deep n-well capacitor, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one skilled in the art that the present invention may be practiced without these specific details or with equivalents thereof. In other instances, well-known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

10

DEEP N-WELL CAPACITOR

Embodiments in accordance with the present invention are described in the context of design and operation of integrated semiconductors. More particularly, embodiments of the present invention relate to systems and methods adding capacitance to integrated circuits. It is appreciated, however, that elements of the present invention may be utilized in other areas of semiconductor operation.

Figure 1 illustrates a side-sectional view of an integrated circuit 100 comprising deep n-well capacitor structure 200, in accordance with embodiments of the present invention.

Integrated circuit 100 comprises a plurality of p-channel field effect transistors (PFETs) and n-channel field effect transistors (NFETs), for example, PFET 110 and NFET 120. PFET 110 comprises source and drain

structures of p+ type material within an n-type well. NFET 120 comprises source and drain structures of n+ type material within p type material, for example, p- epitaxial material or surface p-wells of a semiconductor wafer.

Deep n wells, e.g., deep n well plate 130, are conventionally disposed to isolate

5 transistors operating at different voltages, for example input/output transistors, e.g., NFET 120. It is appreciated that deep n well 130, along with n-well regions 131 and 132, isolate NFET 120 from the epitaxy ground region of the semiconductor wafer.

10 It is appreciated that a capacitor is formed in a diode depletion region between n type and p type material. If such a capacitive structure is coupled between Vdd and ground, additional power supply decoupling can be provided on the integrated circuit.

15 Deep n well capacitor 200 is formed via a deep n well process, e.g., at the same depth and implant energy as deep n well plate 130. In contrast to the conventional art, however, the deep n well region of deep n well capacitor 200 should be segmented into many small regions, or sub structures, to provide connectivity between epitaxy (or bulk p) disposed beneath the deep n wells and

20 the bodies of NFETs formed above the deep n wells. Also in contrast to the conventional art, deep n well capacitor 200 is coupled between Vdd and ground to supply on-chip decoupling capacitance.

It is to be appreciated that an effective capacitor exists between deep n well regions of deep n well capacitor 200, surface p wells and epitaxy p-

material, between deep n well regions deep n well capacitor 200 and bulk p+ material, depending upon depth of the n well(s), and between deep n well regions deep n well capacitor 200 and any p wells or deep p wells.

5 Advantageously, deep n well capacitor 200 does not consume chip surface area. For example, the surface of the integrated circuit can be used for wiring, contacts and FET circuits. For example, when deep n well capacitor 200 crosses beneath an n well, e.g., n well 134, it is coupled to the n well due to the similar doping of the n well and deep n well structures. N wells are typically
10 coupled to Vdd. Hence, deep n well capacitor 200 is coupled to Vdd.
Advantageously, this coupling does not require wiring channels, contact structures or the like, nor does the coupling deleteriously diminish integrated circuit surface area.

15 Similarly, the ground coupling of deep n well capacitor 200 is provided through the p-wells and/or p- type epitaxy. It is appreciated that embodiments in accordance with the present invention are well suited to non-epitaxy wafers. For example, in the absence of p- epitaxy, deep n well capacitor 200 would
20 parasitically couple to bulk p material as well as the p-wells. Epitaxy and/or bulk material are typically coupled to ground. Advantageously, this coupling also does not require wiring channels, contact structures or the like, nor does the coupling deleteriously diminish integrated circuit surface area.

It is to be appreciated that embodiments in accordance with the present invention are well suited to other well known forms of coupling to deep n wells, for example, contact structures.

5 Advantageously, typical layout rules utilized in the construction of deep n well layers are substantially relaxed in comparison to, for example, gate poly, contact and/or metal layers. As a beneficial consequence, the mask for a deep n well layer is relatively inexpensive, as is the incremental processing cost for adding a deep n well layer. Further, the addition of a deep n well layer has a
10 negligible effect on process yield. Consequently, embodiments in accordance with the present invention can be added to an integrated circuit for very low cost.

15 Deep n well capacitor 200 comprises a plurality of sub structures, e.g., deep n well sub structures 210, 220, 230 and 240.

20 In a plan view, the deep n well sub structures may take a variety of shapes, for example, stripes, grids or meshes. In general, such sub structures should be parallel. However, they can cross or intersect. These shapes can be regular or irregular, making turns, etc., to avoid features, for example, a solid deep n well used for isolation, e.g., deep n well plate 130, or to make contact with an n well coupled to a desired voltage, e.g., n well 134. It is desirable to design and construct the gaps between deep n well sub structures wide enough that the gaps do not close under bias conditions. These gaps can supplement
25 the lateral connection from the NFET bodies to the surface taps.

Optional separation p well 290 can be at substantially the same depth as, and between deep n well sub structures 230 and 240. Optional separation p well 290 can be used to increase the capacitance of deep n-well capacitor 200. Separation p well 290 can be used to increase coupling between epitaxy regions and NFET bodies. Separation p well 290 also reduces the separation required between deep n well sub structures 230 and 240 such that the gaps do not close under bias conditions. It is appreciated that separation p well 290 is not required. However, if separation p well was desired, a similar p well 10 structure would typically be located in gaps between most deep n well sub structures.

It is to be appreciated that embodiments in accordance with the present invention are contrary to conventional uses of deep n well. Generally, 15 semiconductor logical and physical design tools, e.g., a design rules checker, enforce a perimeter of n wells around, and coupled to deep n well structures. For example, deep n well plate 130 surrounded by n wells 131 and 132, is compatible with conventional design tools. In contrast, sub structures of deep n well capacitor 200, in general, should not have a perimeter of n wells; rather 20 they are substantially surrounded by p type material. For example, as described previously, it is desirable to have p material between deep n well capacitor sub structures to provide connectivity between epitaxy (or bulk p) and the bodies of NFETs. It is appreciated that deep n well capacitor sub structures should contact n wells somewhere, for conductivity reasons as 25 described previously.

Within a semiconductor design, deep n well plates used conventionally for isolation should be given a unique logical identification. Likewise, deep n well capacitors should be given unique logical identifications. From a logical 5 perspective, deep n well capacitors should not be shorted to other deep n well structures. In general, physical design rules checking should be adjusted to allow non-contiguous deep n well structures to be at the same potential and not enforce an n well perimeter on certain deep n well structures.

10 Figures 2A and 2B illustrate multiple layers of deep n well capacitors, in accordance with embodiments of the present invention. A “deeper” n well can be formed using a different ion implant energy than that which formed a first n well.

15 Figure 2A illustrates using the same mask to form both a first and a second deep n well, in accordance with embodiments of the present invention. Deep n well capacitor 300 is formed separated from and beneath a deep n well layer comprising deep n well capacitor 200 and deep n well plate 130. For example, deep n well sub structures 310 – 340 are disposed directly beneath 20 the corresponding deep n well sub structures 210 – 240. Likewise, a deep n well plate 350 is formed beneath deep n well plate 130. An implant of intermediate energy forms interlayer coupling 315, which couples deep n well capacitor 200 to deep n well capacitor 300. It is appreciated that in this exemplary embodiment, deep n well plate 350 is not coupled to deep n well 25 plate 130, since deep n well plate 130 is coupled to a Vio voltage rather than

Vdd. Using the same mask to form a second deep n well capacitor beneficially simplifies the physical design of the second deep n well capacitor and reduces mask costs.

5 Figure 2B illustrates a more optimal second deep n well layer formed using a different mask than a first deep n well layer, in accordance with embodiments of the present invention. Deep n well capacitor 360 comprises a plurality of sub structures optimized to maximize the capacitance of deep n well capacitor 360. More specifically, the region beneath deep n well plate 130 is divided into multiple deep n well regions to increase surface area of the deep n well capacitor sub structures. For example, the projection of deep n well plate 130 is divided into deep n well capacitor sub structures 361, 362 and 363, with intervening epitaxy.

15 Alternatively, in accordance with other embodiments of the present invention, numerous aspects of the layout of a second deep n well layer can be changed when using a different mask to form the second layer. For example, if a first deep n well capacitor is formed comprising “horizontal” stripes, a second deep n well capacitor can be formed comprising “vertical” stripes at a different 20 depth (or layer) of the integrated circuit. Interlayer couplings could be formed where the stripes “overlap,” forming a lattice of n type material within the epitaxy. It is to be appreciated that interlayer couplings contribute additional capacitance.

Capacitance of multiple deep n well capacitors can be increased by interposing deep p well layer 370 between layers of deep n well, e.g., between n well capacitor 200 and n well capacitor 360. Deep p well layer 370 can advantageously utilize design rules that are relaxed relative to the deep n well 5 regions. For example, p well layer 370 can comprise relatively large, plate-like structures.

In this manner, a variety of layers of deep n well capacitors can be formed, enabling the addition of significant amounts of capacitance to an 10 integrated circuit for very small incremental design and manufacturing costs. Beneficially, the addition of such capacitances enables valuable increases in the maximum operating frequency of integrated circuits. Such faster operation is highly desirable and commands a premium price in the marketplace.

15

It is to be appreciated that deep n well capacitors may be coupled to voltages other than Vdd and ground, in accordance with embodiments of the present invention. Deep n well capacitors may be utilized for virtually any capacitive requirement on an integrated circuit, including within analog 20 circuits, e.g., to produce an RC time constant.

Figure 3 illustrates a flow chart for a method 400 of high frequency operation in an integrated circuit, in accordance with embodiments of the present invention.

25

In block 410, charge stored in a capacitor is accessed. The capacitor comprises a plurality of deep n well regions formed in an epitaxy region of the integrated circuit.

5 In block 420, the charge is coupled to a transistor device of the integrated circuit enabling switching at the high frequency. As previously discussed, highly integrated semiconductor devices, e.g., microprocessors, are limited to a maximum frequency of operation that is in large part limited by transient current capabilities of the integrated circuit packaging.

10 In this manner, charge required by switching transistors of an integrated circuit is accessed from an on-chip charge reservoir. Low inductance coupling between such on-chip charge reservoir(s), e.g., capacitors, and the switching transistors enables higher frequency operation of the 15 integrated circuit than would otherwise be obtainable utilizing conventional systems and methods.

Embodiments in accordance with the present invention, deep n-well capacitor, are thus described. While the present invention has been described 20 in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.